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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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8791	7590	05/19/2005	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			RUTTEN, JAMES D	
			ART UNIT	PAPER NUMBER
			2192	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/002,060	CABOT ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	J. Derek Ruttent	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 30 December 2004.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-28 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-28 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 31 October 2001 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
     1. Certified copies of the priority documents have been received.  
     2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
     3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

## DETAILED ACTION

1. Acknowledgement is made of Applicant's amendment dated 30 December 2004, responding to the 2 September 2004 Office action provided in the rejection of claims 1-28, wherein claims 22 and 25 have been amended, no claims have been canceled, and no new claims have been added. Claims 1-28 remain pending in the application and have been fully considered by the examiner.

2. Applicant has primarily argued that the claims are not anticipated by the Rivin reference because it does not disclose data sampling. This argument is not persuasive, as will be addressed under the *Response to Arguments* section below.

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

*Response to Arguments*

4. The rejection of claims 1, 6, and 7 under 35 USC § 102(e) as being anticipated by US Patent 6,718,286 to Rivin et al. (hereinafter “Rivin”) is discussed on page 7 through the top of page 9 of the amendment.

5. On page 7 and on the top of page 8, with respect to claim 1, applicant essentially argues that Rivin discloses sampling the processor’s program counter, and thus does not disclose data sampling. In response, it is noted that the features upon which applicant relies (i.e., data does not include data sampled from a processor’s program counter) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

6. In the middle of page 8, with respect to claim 1, applicant essentially argues that Rivin discloses sampling the program counter “at random intervals”, but does not teach that the period between samples is random. However, this argument is not clear. It is not understood how a random interval is not the same as a random period. An inter-sample period, as recited in the claim, is interpreted to refer to the period, or interval, between samples. If sampling occurs randomly, wouldn’t that mean that the period between samples must also be random?

7. At the bottom of page 8, with respect to claim 6, applicant essentially argues that Rivin’s SAMPLE and DISABLE signals do not teach resetting hardware. However, the cited passage shows that the data gathering hardware is started in connection with the use of the signals. Furthermore, Figure 1, shows the sampling device including a latch 24 which is connected to a

register 16 which collects the contents of the program counter. The data gathering hardware is effectively reset upon the application of the SAMPLE signal 36, which acts as the latch enable signal, and is also routed to register 16 as the DISABLE signal. Since the application of these signals results in the initialization and collection of data, these are interpreted as resetting the data gathering hardware. Thus, the argument is not convincing.

8. At the bottom of page 8 through the top of page 9, with respect to claim 7, applicant argues: "At most, Rivin et al. start and stop the actual collection of the PC register. However, at no time do Rivin et al. teach the start (or reset) or stop of the hardware." These two statements appear to be at odds with each other, since a PC register *is* hardware. Thus the argument is not convincing.

9. The rejection of claims 20, 25, and 26 under 35 USC § 102(a) as being anticipated by Applicants' Background description (hereinafter "the background section") is discussed on page 9.

10. In response to applicant's argument regarding the background section, that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "more accurate data samples") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

11. Near the bottom of page 9, with respect to claims 25 and 26, applicant essentially argues that the background section does not disclose an inter-sample period. However, the background

section provides an inter-sample period on page 2 lines 13-15: “sampling period, i.e., the time between the taking of samples.” Thus, the argument is not convincing.

12. The rejection of claims 2-5 and 8 under 35 USC § 103(a) as being unpatentable over Rivin in view of US Patent 5,768,500 to Agrawal et al. (hereinafter “Agrawal”) is discussed on pages 10-11.

13. At the top of page 10, applicant argues that Agrawal does not teach the generation of an inter-sample count. However, the generation of an inter-sample count is inherent in the existence of any such count. If a count were not generated, how could it exist?

14. In the second paragraph on page 10, with respect to claim 3, the applicant essentially argues that Rivin does not disclose operations performed during the inter-sample period. However, as cited in the Office Action, column 6 lines 54-60 describe such inter-sample operations: “Sampled program counter contents may be fed back to the host via the ICE...” Again referring to Figure 1, after collecting the sample, the contents of latch 24 are shifted into register 28. As can be seen from the TCLK signal, register 28 is active when latch 24 is inactive. In other words, register 28 operates during the inter-sample period. Therefore, any overhead associated with the sample is accomplished during the inter-sample period.

15. At the bottom of page 10, with respect to claims 4 and 5, applicant essentially argues that Rivin could sample in the cycle following the cycle required to process the sample. However, further inspection of Rivin column 6 lines 50-53 reveals a variable inter-sample period: “The host may usefully call for sampling over an interval, wait an interval and then sample again for

an interval, each of those intervals being one or more (not necessarily uniform in amount) processor clock cycles in duration.”

16. Applicant's arguments at the top of page 11 with respect to claim 8 fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

17. The rejection of claims 9 and 10 under 35 USC § 103(a) as being unpatentable over Rivin in view of Agrawal further in view of U.S. Patent 3,700,869 to Low et al. (hereinafter “Low”) is discussed on page 11. Applicant’s arguments in paragraph 3 on page 11 are based on prior arguments regarding claim 2, addressed above. Thus, these arguments are not convincing.

18. The rejection of claims 11 and 16 under 35 USC § 103(a) as being unpatentable over Rivin in view of U.S. Patent 6,070,009 to Dean et al. (hereinafter “Dean”) is discussed on page 11. Applicant’s arguments in paragraph 5 on page 11 are based on prior arguments regarding Rivin, addressed above. Thus, these arguments are not convincing.

19. The rejection of claims 12-15 and 17 under 35 USC § 103(a) as being unpatentable over Rivin, Dean, and Agrawal is discussed on page 11. Applicant’s arguments are based on prior arguments regarding claims 2-5, 8, 11 and 16, addressed above. Thus, these arguments are not convincing.

20. The rejection of claims 18 and 19 under 35 USC § 103(a) as being unpatentable over Rivin, Dean, Agrawal, and Low is discussed on page 11. Applicant's arguments in the last paragraph on page 11 are based on prior arguments regarding claims 9-11 and 16, addressed above. Thus, these arguments are not convincing.

21. The rejection of claim 21 under 35 USC § 103(a) as being unpatentable over the background section and Agrawal is discussed on page 12. Applicant's arguments are based on prior arguments regarding claims 11, 16, 20, 25, and 26, addressed above. Thus, these arguments are not convincing.

22. The rejection of claims 22-24 under 35 USC § 103(a) as being unpatentable over the background section in view of Agrawal and further in view of "Interrupts" by Daqarta (hereinafter "Daqarta") is discussed on page 12.

23. In the third paragraph on page 12, applicant essentially argues that Daqarta does not teach running an application during the inter-sample period. However, this argument is moot since this new limitation is disclosed by the background section (see page 1 lines 17-20).

24. In the fourth paragraph on page 12, with regard to claim 23, applicant essentially argues that a system cannot process overhead while running an application. However, applicant has not provided any technical reasons why this cannot take place. In fact, a system can process overhead while running an application. See Daqarta page 2 paragraph 1: "As soon as the CPU is able (which is usually 'real soon'), it looks the other way while the **DMA controller moves the sample directly into memory without the CPU even knowing about it**, taking the absolute

minimum amount of time.” In this passage, the DMA controller moves the sample while the CPU continues executing an application.

*Drawings*

25. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the running of the application during the inter-sample period (claim 22), and the dependency of the inter-sample period upon the starting and ending of data gathering hardware (claim 25) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

26. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

27. Claims 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

28. Claim 25 recites “wherein starting the data gathering hardware after the inter-sample period is to end the inter-sample period.” If the data gathering hardware is started *after* the inter-sample period, this implies that the inter-sample period has already ended. If the inter-sample period is already ended, how can starting the data gathering hardware end it again? Further, the use of the word “wherein” suggests that the following text (“starting the data gathering hardware after the inter-sample period”) has already been recited and is being further described. As such, this appears to be a lack of antecedent basis. For the purpose of further examination, this limitation will be interpreted as --wherein starting the data gathering hardware is to end the inter-sample period--.

29. Claim 26 is rejected as being dependent upon a rejected base claim.

***Claim Rejections - 35 USC § 102***

30. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

31. Claims 1, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,718,286 to Rivin et al. (hereinafter "Rivin").

The detailed rejections of claims 1, 6 and 7 are maintained from the prior Office Action and are reproduced below.

As per claim 1, Rivin discloses:

*A method of sampling data* (column 8 line 64 – column 10 line 10), *comprising:*  
*gathering a first data sample during execution of a program; executing the*  
*program during a random inter-sample period; and gathering a second data sample*  
*following the inter-sample period* (column 2 lines 21-24): "The foregoing needs  
are addressed, and advantages obtained, by the use of a  
statistical profiling method which non-intrusively **samples**  
the processor's program counter in a **random** manner." The  
technique of profiling with sampling inherently provides execution of a program between  
the gathering of samples, otherwise program data would not be available for profile  
analysis.).

As per claim 6, the above rejection of claim 1 is incorporated. Rivin further  
discloses: *wherein gathering the first data sample comprises: resetting data gathering*

*hardware, executing the program during a sampling period; and stopping the data gathering hardware at the end of the sampling period* (column 5 lines 36-46: Comment:  
Data gathering hardware is reset using the SAMPLE and DISABLE signals, the sample is collected, and the hardware is stopped through the removal of the signal).

As per claim 7, the above rejection of claim 1 is incorporated. Rivin further discloses: *wherein gathering the first data sample comprises: starting data gathering hardware, executing the program during a sampling period; and stopping the data gathering hardware at the end of the sampling period* (column 5 lines 36-46: Comment:  
Data gathering hardware is started using the SAMPLE signal, the sample is collected, and the hardware is stopped through the removal of the signal).

32. Claims 20, 25, and 26 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Background description appearing on pages 1 and 2 of the originally filed specification (hereinafter referred to as "the background section").

The detailed rejections of claim 20 is maintained from the prior Office Action and is reproduced below.

As per claim 20, the background section discloses:  
*An apparatus for sampling data (page 1 lines 9-16), a memory that stores executable instructions; and a computer processor that executes the instructions (page 1*

lines 9-11: "computer processor executing an application" Comment:

Applications are inherently provided to processor hardware from a memory storage

location, otherwise it would be necessarily be implemented within the hardware itself.)

to:

*gather a first data sample during execution of an application; and gather a second data sample following an inter-sample period* (page 1 lines 17-21:

"Generally, to obtain a sample of data, a sampling program interrupts the application being executed by the computer processor and then executes the sampling program **to obtain a data sample**. The sampling program is **executed several times** to obtain a set of data samples." Also page 2 lines 13-15:

"One way of reducing sampling overhead is to increase the **sampling period**, i.e., the time between the taking of samples.").

### *Claim Rejections - 35 USC § 103*

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

34. Claims 2-5, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivin as applied to claim 1 above, and further in view of U.S. Patent 5,768,500 to Agrawal et al. (hereinafter referred to as “Agrawal”).

The detailed rejections of claims 2-5 and 8 are maintained from the prior Office Action and are reproduced below.

As per claim 2, the above rejection of claim 1 is incorporated. Rivin does not expressly disclose: *generating an inter-sample count; and decrementing the inter-sample count to zero before gathering the second data sample.*

However, in an analogous environment, Agrawal teaches the use of an event detector that triggers an interrupt for sampling when a count reaches a certain value (column 2 lines 37-41; also column 8 lines 26-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Agrawal’s counter with Rivin’s random sampling method. One of ordinary skill would have been motivated to implementing a systematic method for generating an interrupt to trigger a sample gathering event.

As per claim 3, the above rejection of claim 2 is incorporated. Rivin further discloses: *performing overhead operations during the inter-sample period* (column 6 lines 54-60).

As per claim 4, the above rejection of claim 3 is incorporated. Rivin further discloses : *wherein the inter-sample count is longer than an execution time required to perform the overhead operations* (column 4 lines 3-6 describes a sequential sampling which inherently requires that the sample is stored before another sample is collected.).

As per claim 5, the above rejection of claim 3 is incorporated. Rivin further discloses: *wherein the overhead operations include at least one of decrementing the inter-sample count, storing a data sample, and performing a calculation based on a data sample* (column 6 lines 54-60).

As per claim 8, the above rejection of claim 7 is incorporated. Rivin does not expressly disclose event counters. However, Agrawal teaches the use of event counter registers (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Agrawal's registers with Rivin's sampling method. One of ordinary skill would have been motivated to track the execution of a program and collect samples based on the frequency of interesting events.

35. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Rivin and Agrawal as applied to claim 2 above, and further in view of U.S. Patent 3,700,869 to Low et al. (hereinafter "Low").

The detailed rejections of claims 9 and 10 are maintained from the prior Office Action and are reproduced below.

As per claim 9, the above rejection of claim 9 is incorporated. Rivin and Agrawal do not expressly disclose a linear feedback shift register.

However, in an analogous environment, Low teaches that a linear feedback shift register can be used to produce a random bit pattern (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Low's teaching of a linear feedback shift register in Agrawal's counter with Rivin's sampling method. One of ordinary skill would have been motivated to use an efficient arrangement for generating a random binary sequence.

As per claim 10, the above rejection of claim 9 is incorporated. Rivin and Agrawal do not expressly disclose primitive trinomials.

However, Low teaches a linear feedback shift register that is characterized by a primitive trinomial (column 1 lines 26-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Low's primitive trinomials corresponding to a linear feedback shift register in Agrawal's counter with Rivin's sampling method. One of ordinary skill would have been motivated to use a binary sequence corresponding to a primitive trinomial since it is a natural characteristic of using a two-tap linear feedback register which provides an efficient arrangement for generating a random binary sequence.

36. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivin in view of U.S. Patent 6,070,009 to Dean et al. (hereinafter "Dean").

The detailed rejections of claims 11 and 16 are maintained from the prior Office Action and are reproduced below.

As per claim 11, Rivin does not expressly disclose: *An article comprising a machine-readable medium that stores machine-executable instructions for sampling data.*

All further limitations have been addressed in the above rejection of claim 1.

However, in an analogous environment, Dean teaches use of a computer program product comprising a computer readable medium storing instructions for sampling data (column 28 lines 43-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Dean's computer program product with Rivin's sampling technique. One of ordinary skill would have been motivated to store and distribute executable code to other users that are interested in execution profiling and sampling.

As per claim 16, the above rejection of claim 11 is incorporated. All further limitations have been addressed in the above rejection of claim 7.

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37. Claims 12-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Rivin and Dean as applied to claim 11 above, and further in view of Agrawal.

The detailed rejections of claims 12-15 and 17 are maintained from the prior Office Action and are reproduced below.

As per claims 12-15, the above rejection of claim 11 is incorporated. All further limitations have been addressed in the above rejections of claims 2-5, respectively.

As per claim 17, the above rejection of claim 16 is incorporated. All further limitations have been addressed in the above rejection of claim 8.

38. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Rivin, Dean and Agrawal as applied to claim 12 above, and further in view of Low.

The detailed rejections of claims 18 and 19 are maintained from the prior Office Action and are reproduced below.

As per claims 18 and 19, the above rejection of claim 12 is incorporated. All further limitations have been addressed in the above rejections of claims 9 and 10, respectively.

39. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over the background section as applied to claim 20 above, and further in view of Agrawal.

The detailed rejection of claim 21 is maintained from the prior Office Action and is reproduced below.

As per claim 21, the above rejection of claim 20 is incorporated. The background section does not expressly disclose: *a decrementing register; generating an inter-sample count; and decrementing the inter-sample count to zero before gathering the second data sample.*

All further limitations have been addressed in the above rejection of claim 2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Agrawal's counter with the sampling method of the background section. One of ordinary skill would have been motivated to implementing a systematic method for generating an interrupt to trigger a sample gathering event.

40. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the background section and Agrawal as applied to claim 22 above, and further in view of prior art of record "Interrupts", Daqarta, DMA, and FIFO, 2001, appearing on the Information Disclosure Statement by Applicant as designation "AR" dated March 31, 2003 (hereinafter "Daqarta").

As per claim 22, the above rejection of claim 21 is incorporated. The background section discloses overhead operations (page 2 lines 6-12). The background section further discloses running an application during the inter-sample period (page 1 lines 17-20). The background section does not expressly disclose overhead operations *during the inter-sample period.*

However, in an analogous environment, Daqarta teaches that overhead operations are performed during an inter-sample period (page 2 paragraph 1 describes a DMA controller that performs overhead operations including sample storage while the CPU continues execution). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Daqarta's teaching of overhead processing with the background section's . One of ordinary skill would have been motivated to store one sample while an application or CPU is running in order to use a minimum amount of time (Daqarta page 2 paragraph 1).

As per claim 23, the above rejection of claim 22 is incorporated. The background section further discloses increasing the time between samples (page 2 lines 13-15; Comment: This inherently requires an inter-sample time longer than overhead execution, since if it was not, then the entire time would be spent on overhead, and no program execution could be accomplished).

As per claim 24, the above rejection of claim 22 is incorporated. The background section further discloses: *perform overhead operations that include instructions for at least one of decrementing the inter-sample count, storing a data sample, and perform a calculation based on a data sample* (page 2 lines 6-12).

41. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the background section of the originally filed specification in view of Rivin.

As per claim 25, the above rejection of claim 20 is incorporated. The background section further discloses: *data gathering hardware* (page 1 lines 12-16), *and wherein the computer processor executes instructions to: start the data gathering hardware, wherein starting the data gathering hardware is to end the inter-sample period; and stop the data gathering hardware to commence the inter-sample period* (page 2 lines 3-6 describe duration of execution of the sampling program which direct the processor to start and stop the data gathering hardware. Further, page 2 lines 13-15 describes an inter-sample period.). However, the background section does not expressly disclose that starting the data gathering hardware ends the inter-sample period while stopping the data gathering hardware starts the inter-sample period. However, Rivin teaches that a latch could be used to sample hardware (Figure 1, element 24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Rivin's teaching of starting hardware with the background's teaching of data gathering hardware that uses an

inter-sample period. One of ordinary skill would have been motivated to provide hardware that controls the timing of samples (Rivin column 2 lines 41-44).

As per claim 26, the above rejection of claim 25 is incorporated. The background section further discloses event count registers (page 1 lines 12-16).

42. Claims 27 and 28 rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the background section and Agrawal as applied to claim 21 above, and further in view of Low.

The detailed rejections of claims 27 and 28 are maintained from the prior Office Action and are reproduced below.

As per claim 27, the above rejection of claim 21 is incorporated. The background section and Agrawal do not expressly disclose: *a linear feedback shift register, and wherein the computer processor executes an instruction to enable the linear feedback shift register to produce a bit pattern that corresponds the inter-sample count.*

However, in an analogous environment, Low teaches that a linear feedback shift register can be used to produce a random bit pattern (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Low's teaching of a linear feedback shift register in Agrawal's counter with the sampling

method disclosed in the background section. One of ordinary skill would have been motivated to use an efficient arrangement for generating a random binary sequence.

As per claim 28, the above rejection of claim 27 is incorporated. The background section and Agrawal do not expressly disclose primitive trinomials.

However, Low teaches a linear feedback shift register that is characterized by a primitive trinomial (column 1 lines 26-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Low's primitive trinomials corresponding to a linear feedback shift register in Agrawal's counter with the sampling method of the background section. One of ordinary skill would have been motivated to use a binary sequence corresponding to a primitive trinomial since it is a natural characteristic of using a two-tap linear feedback register which provides an efficient arrangement for generating a random binary sequence.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571) 272-3703. The examiner can normally be reached on T-F 6:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2192

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jdr

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PRIMARY EXAMINER